FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: **202841US2PCT**

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 09/762297

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/ES00/00151	**26 April 2000**	**08 June 1999**

TITLE OF INVENTION

DESIGN FOR ELECTRONIC COMPONENT PATTERNS OVER 400 MICRON LAYERS ON PRINTED CIRCUITS

APPLICANT(S) FOR DO/EO/US

Joan Maria BOIXADERA FERRER

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☐ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

Request for Consideration of Documents Cited in International Search Report
Notice of Priority
Drawings (1 Sheet)

JC05 Rec'd PCT/PTO 0 8 FEB 200

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/762297	PCT/ES00/00151	202841US2PCT

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☒ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	$1,000.00	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	$860.00	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	$710.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	$690.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	$100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =		$1,000.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☒ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).		$130.00

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	2 - 20 =	0	x $18.00	$0.00	
Independent claims	1 - 3 =	0	x $80.00	$0.00	
Multiple Dependent Claims **(check if applicable)**.			☐	$0.00	
TOTAL OF ABOVE CALCULATIONS			=	$1,130.00	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable)**.			☐	$0.00	
SUBTOTAL			=	$1,130.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	$0.00	
TOTAL NATIONAL FEE			=	$1,130.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☐	$0.00	
TOTAL FEES ENCLOSED			=	$1,130.00	
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of **$1,130.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **15-0030** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

22850

WILLIAM E. BEAUMONT
REGISTRATION NUMBER 30,996

SIGNATURE

Marvin J. Spivak
NAME

24,913
REGISTRATION NUMBER

February 8, 2001
DATE

DESIGN FOR ELECTRONIC COMPONENT PATTERNS OVER 400 MICRON LAYERS ON PRINTED CIRCUITS

More specifically, the invention refers to a widening of the contact areas arranged on printed circuits and of their conducting zones to receive the conducting parts of the electronic components to be incorporated on said printed circuit.

Known printed circuits consist of a substrate of dielectric material, over which the corresponding conducting material tracks are printed, such as copper, aluminium or similar. Over said printed circuit, the corresponding electronic components are incorporated later, which the printed circuit requires to serve the entrusted purposes. For the latter and between the conducting material tracks, adhesive material is deposited, which permits the electronic components to be supported on the same, previously applied to the copper to be involved in the wave soldering process without them falling before being soldered, which occurs at the ends of the conducting parts, hence completing the process of incorporation of said components on the printed circuits.

Said process is conventional and used in the electronics industry and implies no special difficulty when working with printed circuits of up to 100 microns of copper on the conducting tracks. However, when the same operation is carried out on said printed circuits with conducting layers greater than 105 microns of copper, this same operation becomes almost impossible when executing it with the current production systems and methods.

To solve this problem and assure the manufacturability of electronic circuits, with conducting tracks of more than 105 microns of copper, a series of new figures has been designed for each one of the components to which a copper

surface has been added intended to support the adhesive drops and hence, compensate the height difference represented by the copper when greater than 105 microns, that is, if the width of the electronic component zones destined to be interlocked with the conducting layer of the printed circuit were of a width a_1, the object of the present application has been designed with a width a_2, since in this way it is possible to deposit in this strip of width a_2, the corresponding adhesive material which previously, was deposited between the conducting areas, as may be seen in the figures, hence permitting that the electronic component remains temporarily stuck to the printed circuit board until reaching the wave soldering stage.

Other details and features of the present patent application will be shown in the description given below, referring to the figures attached to this specification where the mentioned details are represented. These details are given as an example, referring to a possible case of a practical embodiment, but not being limited to the details indicated herein. Therefore, this description should be considered as an illustration and without limits.

Below, there is a detailed list of the components mentioned in the present patent application, (10) printed circuit, (11) material substrate, (12) conducting material track, (13) electronic component, (13.1) electronic part, (13.2) conducting part, (14) adhesive, (15) solder.

Figure 1 is a simplified front elevation view of a printed circuit board (10) with a copper track (12) less than 105 microns thick, over which an electronic component (13) should be incorporated, applying an adhesive (14) between the copper tracks (12).

Figure 2 is a similar view to that of figure number 1, but at a later stage, that is, when incorporating the electronic component (13) to the copper track (12) and being interlocked to the same with a help of the adhesive (14) and later on is soldered by conventional methods and the soldering

material deposited, such as tin or similar (15), said electronic component (13) being mechanically and electrically incorporated to the printed circuit board (10).

Figure 3 is a simplified front elevation view similar to figure 1, but when the copper track or conducting material has a height of h_2 instead of h_1.

Figure 4 is a front elevation view similar to figure 3, in which the conducting part (12) has been widened by (a_2-a_1) with the purpose that when it is desired to incorporate an electronic component (13) the adhesive (14) does not spill over the conducting part.

Figure 5 is a front elevation view similar to figure 3, but at a later moment when the electronic component (13) has been duly interlocked and soldered to the copper track (12) at a thickness greater than 105 microns and height h_2.

In one of the preferred embodiments of the object of the present application, which may be seen in figures number 3 and 4, when it is wished to incorporate an electronic component (13) to a printed circuit board (10) and when the latter is formed by a copper track or conducting material whose thickness h_2 is greater than 105 microns, the conventional methods indicated in figures 1 and 2 are not possible, that is, as a consequence of the difference of height of h_2 compared with h_1, a drop of glue (14) with a very large diameter should be incorporated, resulting in part of it being spilled over the layer (12) and being irregularly distributed over the zone (13.2) or conducting part of the electronic component which should be soldered later on, as may be seen in figure 3.

To prevent these drawbacks, some pads have been designed, that is, some zones to tint or receive a layer of adhesive with a greater surface, so that if in a conventional component, it were a_1, with the new design it is a_2; see figure 5, that is, greater than a_1 and as a result, the adhesive may be directly deposited on this area of the

conducting layer or copper track (12), so that it is interlocked to the electronic component (13) to later on receive the solder (15) by conventional methods.

Concluding, the invention is reduced to an increase of width of the pads of the electronic components (13), hence able to permit the deposition of the adhesive drops on the conducting layer (12) and in this way, compensate the height difference of the copper track when this is greater than 105 microns.

Having sufficiently described the essence of the present patent application, according to the attached drawings, it is understood that any modifications may be introduced, as relevant, provided they do not alter the essence of the present patent, being summarised in the following claims.

C L A I M S

1.- "DESIGN FOR ELECTRONIC COMPONENT PATTERNS OVER 400 MICRON LAYERS ON PRINTED CIRCUITS", consisting of a dielectric material substrate (11) over which, the conducting material tracks (12) are drawn and constructed, such as copper, aluminium or similar, depositing between said tracks (12) an adhesive material (14) with the purpose of interlocking to electronic components (13) as a preliminary step, so that once they are adhered to the conducting material track (12), they receive the corresponding soldering material (15) in a wave soldering process, characterised in that in the printed circuits (10) the layer of conducting material or copper track (12) will be h_2 greater than h_1 and the corresponding pads of width a_1 will have a greater width a_2.

2.- "DESIGN FOR ELECTRONIC COMPONENT PATTERNS OVER 400 MICRON LAYERS ON PRINTED CIRCUITS" in accordance with claim 1, characterised in that the conducting parts (13.2) of electronic components (13) will have a width a_2 when the copper conducting layers (12) have a height h_2 greater than 105 microns.

ABSTRACT

In order to ensure manufacturability of electronic circuits with conductor strips having a copper width of over 105 microns, a new series of patterns has been designed for each of the components. A copper surface has been added to said components to receive the adhesive drops thereby compensating for the height difference if the copper surface is bigger than 105 microns. If the width of the areas of the electronic component which are to be connected to the conductive coating of the printed circuit had a width a1, the width according to the invention is now a2, thereby making it possible to deposit the corresponding adhesive material in said strip having width a2.

1/1

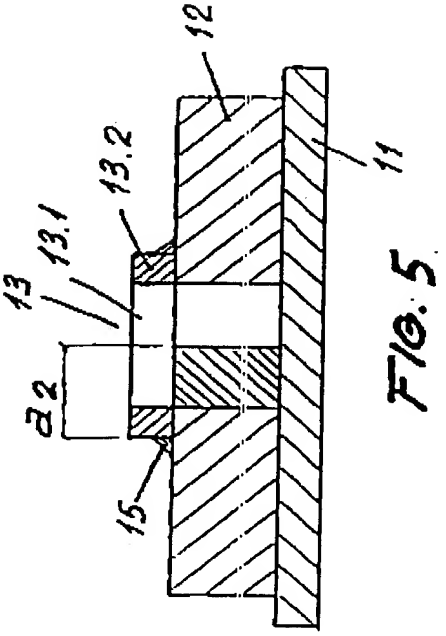

FIG. 5

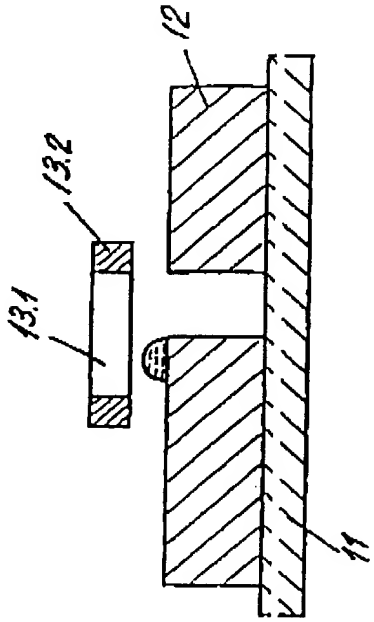

FIG. 4

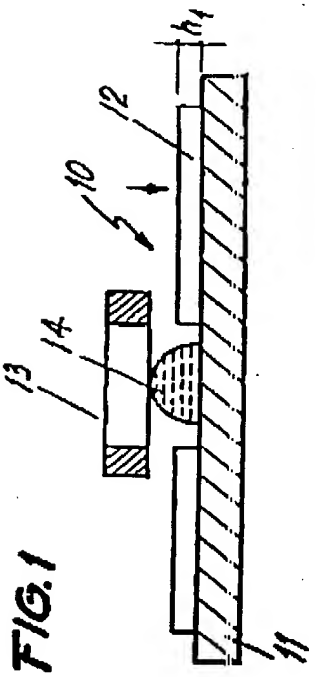

FIG.1

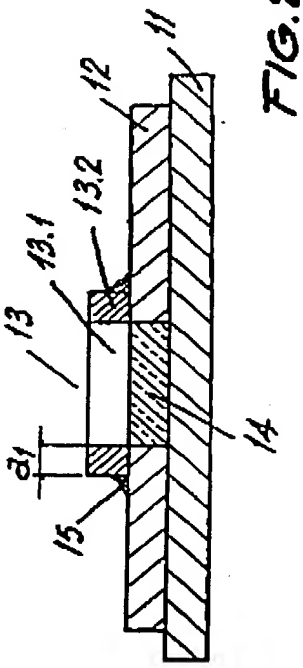

FIG.2

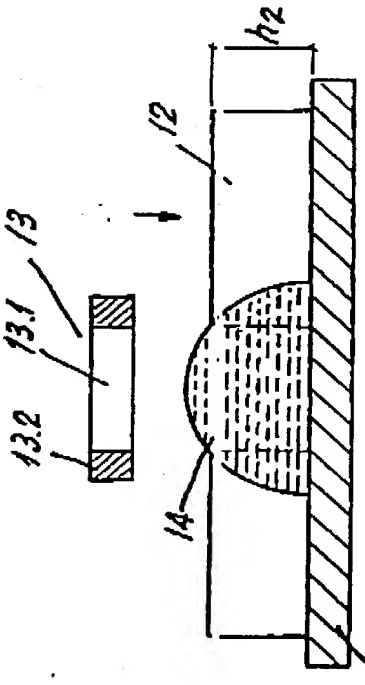

FIG.3

Declaration, Power Of Attorney and Petition

WE (I) the undersigned inventor(s), hereby declare(s) that:

My residence, post office address and citizenship are as stated below next to my name,

We (I) believe that we are (I am) the original, first, and joint (sole) inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DESIGN FOR ELECTRONIC COMPONENT PATTERNS OVER 400 MICRON LAYERS ON PRINTED CIRCUITS

the specification of which

☐ is attached hereto.

☒ was filed on February 8, 2001 as

Application Serial No. 09/762,297

and amended on _____.

☒ was filed as PCT international application

Number PCT/ES00/00151

on April 26, 2000,

and was amended under PCT Article 19

on _____ (if applicable).

We (I) hereby state that we (I) have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

We (I) acknowledge the duty to disclose information known to be material to the patentability of this application as defined in Section 1.56 of Title 37 Code of Federal Regulations.

We (I) hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed. Prior Foreign Application(s)

Application No.	Country	Day/Month/Year	Priority Claimed
P 9901256	SPAIN	08 June 1999	☒ Yes ☐ No
			☐ Yes ☐ No
			☐ Yes ☐ No
			☐ Yes ☐ No

We (I) hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

We (I) hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

Application Serial No.	Filing Date	Status (pending, patented, abandoned)
PCT/ES00/00151	26 April 2000	

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And we (I) hereby appoint: Norman F. Oblon, Reg. No. 24,618; Marvin J. Spivak, Reg. No. 24,913; C. Irvin McClelland, Reg. No. 21,124; Gregory J. Maier, Reg. No. 25,599; Arthur I. Neustadt, Reg. No. 24,854; Richard D. Kelly, Reg. No. 27,757; James D. Hamilton, Reg. No. 28,421; Eckhard H. Kuesters, Reg. No. 28,870; Robert T. Pous, Reg. No. 29,099; Charles L. Gholz, Reg. No. 26,395; William E. Beaumont, Reg. No. 30,996; Jean-Paul Lavalleye, Reg. No. 31,451; Stephen G. Baxter, Reg. No. 32,884; Richard L. Treanor, Reg. No. 36,379; Steven P. Weihrouch, Reg. No. 32,829; John T. Goolkasian, Reg. No. 26,142; Richard L. Chinn, Reg. No. 34,305; Steven E. Lipman, Reg. No. 30,011; Carl E. Schlier, Reg. No. 34,426; James J. Kulbaski, Reg. No. 34,648; Richard A. Neifeld, Reg. No. 35,299; J. Derek Mason, Reg. No. 35,270; Surinder Sachar, Reg. No. 34,423; Jeffrey B. McIntyre, Reg. No. 36,867; William T. Enos, Reg. No. 33,128; Michael E. McCabe, Jr., Reg. No. 37,182; Bradley D. Lytle, Reg. No. 40,073; and Michael R. Casey, Reg. No. 40,294; our (my) attorneys, with full powers of substitution and revocation, to prosecute this application and to transact all business in the Patent Office connected therewith; and we (I) hereby request that all correspondence regarding this application be sent to the firm of OBLON, SPIVAK, McCLELLAND, MAIER & NEUSTADT, P.C., whose Post Office Address is: Fourth Floor, 1755 Jefferson Davis Highway, Arlington, Virginia 22202.

We (I) declare that all statements made herein of our (my) own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1-00

Joan Maria BOIXADERA FERRER
NAME OF FIRST SOLE INVENTOR

Signature of Inventor

✓ 07-02-01
Date

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